REMARKS

Claims 1, 2, 6, 8-14, 18 and 19 are active. Claims 3 – 5, 7 and 15-17 are canceled. Claims 1, 2, 4 and 6-19 are rejected under 35 USC 102 as anticipated by Arai pub. US application '75093.

Amended claims 1, 2, 6, 8-14, 18 and 19 are presented for the Examiner's reconsideration.

Amended claim 1 calls for:

> a substrate;
>
> a patterned electrically conductive electrode lower layer on and contiguous with a surface of the substrate, the lower layer being formed as a plurality of spaced apart sets of electrodes wherein each set comprises spaced apart source/drain electrodes;
>
> an arrangement on and contiguous with a region of the substrate located between at least two of the sets of said electrodes, the arrangement for precluding the wetting of that substrate region by a subsequently applied organic functional semiconducting layer and to thereby minimize current leakage between the two sets of electrodes; and
>
> a patterned functional organic semiconductor layer on, over and contiguous with the at least two sets of electrodes and on, over, and contiguous with the substrate surrounding the at least two sets of the electrodes to thereby embed the at least two sets of electrodes in the semiconductor layer wherein there is substantially no semiconductor layer overlying or contiguous with the substrate in said region of the substrate

This structure is distinguishable over Arai and is not disclosed or suggested therein. The claim calls for the source and drain electrodes to be on and contiguous with the substrate surface. This is not disclosed by Arai who discloses an insulator layer 103 on the substrate and not electrodes as claimed. This alone is different than amended claim 1 which also calls for more.

The claim also calls for an arrangement on and contiguous with a region of the substrate located between at least two of the sets of said electrodes, the arrangement for precluding the wetting of that substrate region by a subsequently applied organic functional semiconducting layer. This is a positively claimed element and not a product by process limitation. The arrangement must be on and contiguous with the substrate. The arrangement is for precluding wetting of the substrate by the later applied semiconducting layer so that this region is substantially free of the semiconducting layer which minimizes

current leakage there across. This is not shown or suggested by Arai. In Arai, the resist layer mask 104 (dashed line Fig. 2B) is on and over the insulation 105 to permit the formation of the insulation pattern by etching (the resist acting as a mask during this etching process). This is different than claim 1 which calls for the arrangement to be on and contiguous with the substrate. In Arai the resist mask 104 is not on and contiguous with the substrate 101.

The claim calls for the drain and source electrodes to be embedded in the later applied semiconductor layer. The semiconductor is over and contiguous with the electrodes and also is on a portion of the substrate. See applicants' Fig. 2. This too is not shown or suggested by Arai. His semiconductor is on insulated film 105 and not on the drain/source electrodes or the substrate as claimed. The semiconductor is not contiguous with the substrate as claimed.

The semiconductor as claimed does not wet the substrate due to the arrangement. In Arai, the semiconductor is not contiguous with the substrate, not due to the arrangement, e.g., the photoresist mask 4, but due to the insulation layer 103 which covers the entire substrate. This too is not what is claimed. The photo resist mask 104 of Arai is irrelevant to the semiconductor not being wetted on the substrate simply because the resist is applied to permit etching the insulation layer 105. After the layer 105 is etched the resist is removed and the semiconductor is then applied over the layer 105 and the electrode 102. The resist has nothing to do with patterning the semiconductor layer. Further the electrode 102 on the substrate is a gate and not source and drain electrodes as claimed. Also there is no suggestion of the solution to the problem of leakage between electrodes due to the semiconductor free area as claimed. Thus Arai is different than and does not anticipate nor suggest amended claim 1.

The arrangement is such to thereby minimize current leakage between the two sets of electrodes. This is not shown or suggested by Arai who does not recognize the current leakage problem when a semiconductor layer engages multiple sets of drain/source electrodes and thus does not suggest providing a region between these electrodes free of the semiconductor layer on the substrate. See applicants' figures, especially figure 1 showing a gap between the drain/source electrodes of the multiple FETs shown. Amended claim 1 is believed allowable.

Claims 6 and 13 call for similar structure as in claim amended claim 1 and are believed allowable over Arai at least for the same or similar reasons.

Claim 10 is a method claim corresponding to claim 1 and is believed allowable for the similar reasons.

The remaining claims depend from the independent claims and are believed allowable for at least the same reasons given for the claims from which they depend.

Since claims 1, 2, 6, 8-14, 18 and 19 have been shown to be in proper form for allowance, such action is respectfully requested.

The Commissioner is authorized to charge any underpayment of fees associated with this communication or credit any overpayment to Deposit Account No. 03-0678.

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